AMENDMENTS

IN THE CLAIMS:

Please cancel claims 33-36.

19. (Previously presented) A method of producing a vertically emitting laser, comprising:

forming a semiconductor layer stack over a substrate; and

processing the semiconductor layer stack, thereby forming a current aperture and a semiconductor relief associated with the vertically emitting laser, wherein an area of the current aperture and an area of the semiconductor relief are defined in a same processing operation.

20. (Previously presented) The method of claim 19, wherein the same processing operation results in the areas of the current aperture and the semiconductor relief to comprise a predetermined size ratio that is substantially self-scaling with respect to processing variations.

21. (Previously presented) The method of claim 20, wherein the same processing operation comprises an oxidation of a plurality of layers within the semiconductor layer stack.

22. (Previously presented) The method of claim 21, wherein the semiconductor layer stack comprises an oxidizable auxiliary layer and an oxidizable current aperture layer, and wherein the oxidation of the plurality of layers within the semiconductor layer stack causes an oxidation of peripheral portions of the oxidizable auxiliary layer and the oxidizable current aperture layer, and wherein the predetermined size ratio is defined by an oxidation rate of the oxidizable auxiliary layer and the oxidizable current aperture layer, respectively.

23. (Previously presented) The method of claim 22, wherein processing the semiconductor layer stack further comprises forming a mesa structure associated with at least a portion of the semiconductor layer stack prior to the oxidation, wherein the oxidizable auxiliary layer and the oxidizable current aperture layer comprise a portion of the mesa structure.

24. (Previously presented) The method of claim 23, wherein the semiconductor layer stack comprises:

the oxidizable current aperture layer overlying the substrate;

at least one semiconductor intermediate layer overlying the oxidizable current aperture layer;

the oxidizable auxiliary layer overlying the at least one semiconductor intermediate layer; and

a covering layer overlying the oxidizable auxiliary layer,

wherein forming the mesa comprises patterning the oxidizable current aperture layer, the at least one semiconductor intermediate layer, the oxidizable auxiliary layer and the covering layer, and

wherein the oxidation results in an oxidation of patterned peripheral portions of the oxidizable current aperture layer and the oxidizable auxiliary layer.

25. (Previously presented) The method of claim 24, further comprising:

removing oxidized portions of the oxidized auxiliary layer, thereby exposing a portion of the underlying at least one semiconductor intermediate layer;

etching the exposed portion of the at least one semiconductor intermediate layer down to a predetermined depth, thereby forming the semiconductor relief therein, wherein the predetermined etch depth corresponds to a height of the semiconductor relief; and

removing the covering layer and a non-oxidized portion of the auxiliary layer, thereby exposing the semiconductor relief.

26. (Previously presented) The method of claim 25, further comprising forming at least one mirror layer over the semiconductor relief.

27. (Previously presented) The method of claim 19, further comprising forming an upper mirror layer overlying the semiconductor layer stack, wherein the semiconductor relief is arranged between the upper mirror layer and the current aperture.

28. (Previously presented) The method of claim 27, wherein the area of the semiconductor relief is greater than the area of the current aperture.

29. (Previously presented) The method of claim 27, wherein forming the upper mirror layer comprises depositing a dielectric layer over the processed semiconductor layer stack.

30. (Previously presented) The method of claim 19, further comprising:

patterning the semiconductor layer stack to form a mesa structure including the current aperture and the semiconductor relief included therein; and

forming an upper electrical contact of the laser on a top portion of the mesa structure,

wherein the upper electrical contact, the current aperture, and the semiconductor relief are arranged relative to one another in a self-aligned manner.

31. (Previously presented) The method of claim 30, wherein the upper electrical contact comprises an intra-cavity contact.

32. (Previously presented) The method of claim 30, wherein patterning the semiconductor layer stack to form the mesa structure comprises exposing apportion of

a semiconductor intermediate layer, and further comprising forming an intra-cavity contact on the exposed portion of the semiconductor intermediate layer.

33-36. (Canceled).

37. (Previously presented) A method of forming a vertically emitting laser, comprising:

forming a base portion comprising a substrate, and a photon generating portion overlying the substrate;

forming an oxidizable current aperture layer over the base portion;

forming a semiconductor intermediate layer over the current aperture layer;

forming an oxidizable auxiliary layer over the semiconductor intermediate layer;

forming a covering layer over the oxidizable auxiliary layer;

forming a first mask over the covering layer;

patterning the covering layer, the oxidizable auxiliary layer, the semiconductor intermediate layer, and the oxidizable current aperture layer using the first mask to form a mesa structure;

oxidizing the mesa structure, thereby causing peripheral portions of the oxidizable current aperture layer and the oxidizable auxiliary layer to become oxidized, and further causing non-oxidized portions of the current aperture layer and the auxiliary layer to be self-aligned and self-scaled with respect to one another;

forming a second mask over the first mask and over the mesa structure, wherein the second mask comprises an annular opening therein;

patterning an annular opening in the first mask, and the covering layer, thereby exposing the oxidizable auxiliary layer that has been partially oxidized about a peripheral portion thereof;

selectively removing the peripheral oxidized portion of the oxidizable auxiliary layer, thereby leaving a substantially non-oxidized, central portion of the auxiliary layer remaining;

etching into an exposed portion of the semiconductor intermediate layer to a predetermined depth, thereby defining a semiconductor relief portion of the semiconductor intermediate layer underlying the central portion of the auxiliary layer, wherein a height of the semiconductor relief is defined by the predetermined depth of the etch of the semiconductor intermediate layer; and

removing the first and second masks, the covering layer, and the central portion of the auxiliary layer, thereby exposing the semiconductor relief.

38. (Previously presented) The method of claim 37, wherein the semiconductor intermediate layer comprises a plurality of layers, and wherein one of the plurality of layers comprises an etch stop layer, wherein etching the exposed portion of the semiconductor intermediate layer continues down to the etch stop layer and substantially stops thereat, and wherein a location of the etch stop layer within the plurality of layers defines the predetermined depth.

39. (Previously presented) The method of claim 37, further comprising forming one or more mirror layers over the semiconductor relief.